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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTENTION: HONORABLE
Commissioner for Patents

P.O. Box 1450

In re the Patent of: **TAKEMORI, Toshiyuki et al.** P.T.O. Confirmation No.: 6603

Patent No. **6,737,704** Issued: **May 18, 2004**

For: **TRANSISTOR AND METHOD OF MANUFACTURING THE SAME**

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop DAC
June 30, 2004

Sir:

The undersigned requests that a Certificate of Correction be issued for the above-identified patent as indicated on the attached Form PTO-1050.

This request is being made in order to correct an error in the claims. In claim 1 some information was omitted and some unrelated information was inserted. Please change claim one to be as it is shown in the Preliminary Amendment filed March 13, 2003(copy enclosed). These errors appear to be inadvertent clerical errors made by the Patent and Trademark Office. It is respectfully submitted that no new matter has been added.

Since this error is a Patent and Trademark Office printing error, it is respectfully submitted that no fee is required.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

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Attorney for Applicant
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MRQ/lp
Atty. Docket No. **001155**
Suite 1000
1725 K Street, N.W.
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23850
PATENT TRADEMARK OFFICE

7 JUL 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKEMORI, Toshiyuki et al.**

Group Art Unit: **2814**

Serial No.: **09/660,439**

Examiner: **Shrinivas (Steven) H. RAO**

Filed: **September 12, 2000**

P.T.O. Confirmation No.: **6603**

For: **TRANSISTOR AND METHOD OF MANUFACTURING THE SAME**

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

March 13, 2003

Sir:

This is a Preliminary Amendment filed along with the Request for Continued Examination (RCE) filed March 13, 2003. Please amend the above-identified application as follows:

IN THE CLAIMS:

Claims 1 and 11 have been amended as follows:

1. (Twice Amended) A transistor comprising:

a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type provided on said semiconductor layer and a conductive region of a second conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided inner surface of said conductive region and exposed on side surface of said trench;

a gate insulating film provided on the side surface of said trench, an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

a source electrode film provided in contact with at least said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material, said source region being substantially square when viewed from a direction parallel to said side surface of said trench, said source electrode film being contiguous and extending from an upper portion of said source region and a side surface of said source region, said contiguous source electrode film covering an opening of said trench in its entirety.

11. (Twice Amended) A transistor comprising:

a semiconductor substrate having a drain layer of a first conductivity type and a conductive region of a second conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided in inner surface of said conductive region and exposed on side surface of said trench;

a gate insulating film provided on the side surface of said trench, an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with said conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material, said source electrode film being contiguous and extending from an upper portion of said source region and a side surface of said source region, said contiguous source electrode film covering an opening of said trench in its entirety,

said source region being substantially square when viewed from a direction parallel to said side surface of said trench; and

a metal film formed on a surface of said drain layer opposite to said conductive region to establish Schottky contact with said drain layer.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: **6,737,704**
DATED : **May 18, 2004**
INVENTOR(S): **TAKEMORI et al.**

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim1;
Column 12 starting on line 13 change
"surface of said source region, said contiguous source electrode film covering a plurality of openings of said trenches in their entireties,

said source region being substantially square when viewed from a direction parallel to said side surface of said trench; and

a metal film formed on a surface of said drain layer opposite to said conductive region to establish Schottky contact with said drain layer."

to be:
-- a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided inner surface of said conductive region and exposed on side surface of said trench;

a gate insulating film provided on the side surface of said trench, an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

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Patent No.:**6,737,704**

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FORM PTO 1050 (REV. 3/82)

7 JUL 2004

JUL 2004

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: **6,737,704**
DATED : **May 18, 2004**
INVENTOR(S): **TAKEMORI et al.**

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

continued from page1

a source electrode film provided in contact with at least said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material, said source region being substantially square when viewed from a directional parallel to said side surface of said trench, said source electrode film being contiguous and extending from an upper portion of said source region and a side surface of said source region, said contiguous source electrode film covering an opening of said trench in its entirety.--

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